REMARKS

In the Official Action mailed **January 29, 2002**, the Examiner reviewed claims 1-20. Claims 1-3, 5-7, and12 were rejected under 35 U.S.C. §102(b) as being anticipated by Dea (USPN 5,469,208, hereinafter "Dea"). Claims 4, 9, 13-17, and 19 were rejected under 35 U.S.C. §103(a) as being unpatentable over Dea in view of Abramatic et al. (USPN 4,546,383, hereinafter "Abramatic"). Claim 10 was rejected under 35 U.S.C. §103(a) as being unpatentable over Dea. Claim 18 was rejected under 35 U.S.C. §103(a) as being unpatentable over Dea and Abramatic as applied to claim 13 and further in view of Hardiman (USPN 5,923,223, hereinafter "Hardiman").

Rejections under 35 U.S.C. §102(b) and §103(a)

Independent claim 1 was rejected as being anticipated by Dea and independent claim 13 was rejected as being unpatentable over Dea in view of Abramatic. Applicant respectfully points out that Dea is directed to a compression/decompression accelerator **coupled to a system bus** (See Dea, Fig. 1). In contrast, the present invention discloses a graphics controller **within a core logic unit** of a computer system (See Fig. 2, and page 7, line 24 to page 8, line 1 of the instant application). A core logic unit is circuitry within a computer system that interfaces a processor to a memory and a peripheral bus and performs other functions (See page 5, lines 7-8 of the instant application). To clarify this distinction, Applicant has amended independent claims 1 and 13 to specify that "the core logic chip is a semiconductor chip that couples the processor to a main memory and a system bus for the computer system." This claim amendment finds support in FIG. 2 of the instant application.

Note that the compression/decompression accelerator described in Dea does not couple the processor to the main memory or to a system bus. Hence,

claims 1 and 13 are presently amended are in condition for allowance. Moreover, claims 2-10, and 12 which depend upon claim 1, and claims 14-19 which depend on claim 13, are for the same reasons in condition for allowance and for reasons of the unique combinations recited in these claims.

Version with markings to show changes made

In The Claims:

1. (Twice Amended) A method for compressing video data in a computer system, comprising:

receiving a stream of data from a current video frame in the computer system;

computing a difference frame from the current video frame and a previous video frame as the current video frame streams into the computer system, wherein computing the difference frame includes computing the difference frame in a core logic chip within the computer system; and

storing the difference frame in a memory in the computer system.

13. (Twice Amended) A method for compressing video data in a computer system, comprising:

receiving a stream of data from a current video frame in the computer system;

computing a difference frame from the current video frame and a previous video frame as the current video frame streams into the computer system, wherein computing the difference frame includes computing an exclusive-OR between the current video frame and the previous video frame, and wherein computing the difference frame includes computing the difference frame in a core logic chip within the computer system;

storing the difference frame in a memory in the computer system;

storing the current video frame in the memory in the computer system; and

compressing the video data using the difference frame to produce compressed video data.

CONCLUSION

It is submitted that the present application is presently in form for allowance. Such action is respectfully requested.

Respectfully submitted,

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